IN THE CLAIMS

Please rewrite claims 1 - 8 as shown in the complete list of claims that is presented below.

1. (currently amended) A semiconductor circuit ~~wherein~~ comprising:

a JTAG (Joint Test Action Group) port;

a flash ROM that stores a security bit;

a TAP (Test Access Port) that communicates with the flash ROM; and

a JTAG control circuit controlled by the security bit of ~~a~~ the flash ~~ROM is equipped~~ ROM, the JTAG control circuit being connected between the JTAG port and ~~a~~ the TAP ~~(Test Access Port).~~ and allowing or preventing communication of signals between the JTAG port and the TAP depending on the state of the security bit.

2. (currently amended) ~~A~~ The semiconductor circuit of claim 1, further comprising:

an inhibit ~~(INHIBIT) NAND gate;~~ gate having first and second input terminals, the first input terminal receiving the security bit from the flash memory;

a micro controller general purpose port; and

a Pin scramble-circuit decoding ~~a~~ the micro controller general-purpose port, ~~which are set between the security bit of a flash ROM and the JTAG control circuit; and~~ the second input terminal of the inhibit gate receiving an output signal from the Pin scramble circuit.

~~a circuit wherein the inverted level of the one of the Pin scramble circuit output is input the one side of the inhibit NAND gate and the output of the security bit of a flash ROM is input the other side of the inhibit NAND gate.~~

3. (currently amended) ~~A~~ The semiconductor circuit of claim 1, further comprising:

an inhibit ~~NAND~~ gate having first and second input terminals, the first input terminal receiving the security bit from the flash memory; and

a micro controller that includes a debug enable ~~(DBG_EN)~~ register as an internal register of the micro controller, ~~which are set between the security bit of a flash ROM and the JTAG control circuit; and~~ the second input terminal of the inhibit gate receiving an output signal of the debug enable register.

~~a circuit wherein the inverted level of the one of the debug enable register output is input the one side of the inhibit NAND gate and the output of the security bit of a flash ROM is input the other side of the inhibit NAND gate.~~

4. (currently amended) A semiconductor circuit having a security releasing means comparing ~~the~~ first data ~~which is input a test port~~ with ~~the~~ second data ~~stored in a memory device~~ and turning on a switch when the two data agree, said ~~the~~ semiconductor circuit comprising:

a memory device to store a control program and ~~data;~~ data, the date stored in the memory device including said first data;

a central processing unit to execute a specific process according to the program;

a non-volatile register that stores said second data, said second data including a security bit;

a test port to input and output test ~~signals;~~ signals, including said first data; and

a ~~switch~~ unit to control on/off between the test port and at least one of the memory device ~~and/or~~ and the central processing unit according to the security bit set in ~~a~~ the nonvolatile ~~register.~~ register, the unit comprising said switch.

5. (currently amended) A semiconductor circuit according to claim 4, wherein the security releasing means ~~comprising:~~ comprises:

an address register keeping ~~the~~ address information input from the test port and specifying ~~the~~ a memory range of the memory device;

a data register keeping ~~the~~ data information input from the test port;

a comparator comparing ~~the~~ data read out from the memory device based on the address information with the data kept in the data register; and

a logic gate turning on ~~a~~ the switch when the two data agree, independent of the state of security bit.

6. (currently amended) A semiconductor circuit according to the claim 4, wherein the security releasing means ~~comprising:~~ comprises:

an address counter counting ~~the~~ timing information input from the test port sequentially and specifying ~~the~~ a memory range;

a data register keeping ~~the~~ data information input from the test port;

a comparator comparing ~~the~~ data read out from the memory device based on the specification of the address counter with the data kept in the data register;

an agreement number counter outputting a releasing signal when the number of agreement of the data comes to the specific value; and

a logic gate turning on ~~a~~ the switch when the releasing signal is output, independent of the state of security bit.

7.(currently amended) A semiconductor circuit according to claim 6, further comprising an address register setting ~~the~~ an initial value based on ~~the~~ address information input from the test port.

8. (currently amended) A semiconductor circuit comprising:

a memory device to store a control program and data;

a central processing unit to execute a specific process according to the program;

a test port to input and output test signals;

a switch to control on/off between the test port and the central processing unit; ~~and~~

a memory device; and

a security releasing means for comparing ~~the~~ data input ~~a~~ via the test port with the data stored in ~~a~~ the memory device and turning on ~~a~~ the switch when the two data agree.